What is claimed as new and desired to be protected by Letters Patent of the United States is:

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1. A data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal;

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective first delayed first clock signal to a respective one of said plurality of output circuits.

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2. A data output apparatus as in claim 1 wherein each of said output circuits has an associated output data hold time, the timing of which is adjusted by the delay of a respective delay circuit.

3. A data output apparatus as in claim 2 wherein the amount of delay applied by each of said adjustable delay circuits is programmable.

4. A data output apparatus as in claim 2 wherein the delay of each of said adjustable delay circuits is adjusted such that the timing of said data hold time of each of said output circuits is substantially coincident.

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5. A data output apparatus as in claim 2 further comprising a plurality of data output terminals respectively connected to said output circuits, and

wherein the delay of each of said adjustable delay circuits is adjusted such that the data hold time as seen at said respective output terminal is substantially coincident.

6. A data output apparatus as in claim 1 wherein each of said delay circuits comprises:

an input for receiving said first clock signal;

a plurality of delay elements, each of said delay elements providing different respective delay to a signal applied thereto; and,

a switch circuit for selectively causing a selected one of said delay elements to delay said first clock signal and apply a delayed first clock signal to a respective output circuit.

7. A data output apparatus as in claim 6 further comprising a programming circuit for programming said switch circuit to selectively apply said first clock signal to one of said delay elements.

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8. A data output apparatus as in claim 7 wherein said programming circuit comprises at least one fuse element.

9. A data output apparatus as in claim 7 wherein said programming circuit comprises at lest one anti-fuse element.

10. A data output apparatus as in claim 6 wherein said switch circuit comprises a plurality of switch elements respectively coupled to said plurality of delay elements, one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element.

11. A data output apparatus as in claim 10 further comprising a programmable circuit for programming which of said switch elements is selectively enabled.

12. A data output apparatus as in claim 1 wherein said output circuits are output buffer circuits.

13. A data output apparatus as in claim 1 wherein each of said output circuits receives and outputs a respective data signal from a memory array.

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14. A data output apparatus as in claim 6 wherein said switch circuit comprises at least one multiplexor.

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15. A processor based system comprising:

a processor; and

at least one memory circuit coupled to said processor, at least one of said processor and memory circuit including a data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal;

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits.

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16. A processor based system as in claim 15 wherein each of said output circuits has an associated output data hold time, the timing of which is adjusted by the delay of a respective delay circuit.

17. A processor based system as in claim 16 wherein the amount of delay applied by each of said adjustable delay circuits is programmable.

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18. A processor based system as in claim 16 wherein the delay of each of said adjustable delay circuits is adjusted such that the timing of said data hold time of each of said output circuits is substantially coincident.

19. A processor based system as in claim 16 wherein each of said output circuits is coupled to a respective output terminal and the delay of each of said adjustable delay circuits is adjusted such that the data hold time as seen at said respective output terminal is substantially coincident.

20. A processor based system as in claim 15 wherein each of said delay circuits comprises:

an input for receiving said first clock signal;

a plurality of delay elements, each of said delay elements providing a different respective delay to a signal applied thereto; and,

a switch circuit for selectively causing a selected one of said delay elements to delay said first clock signal and apply a delayed first clock signal to a respective output circuit.

21. A processor based system as in claim 20 further comprising a programming circuit for programming said switch circuit to selectively apply said first clock signal to one of said delay elements.

22. A processor based system as in claim 21 wherein said programming circuit comprises at least one fuse element.

23. A processor based system as in claim 21 wherein said programming circuit comprises at lest one anti-fuse element.

24. A processor based system as in claim 21 wherein said switch circuit comprises a plurality of switch elements respectively coupled to said plurality of delay elements, one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element.

25. A processor based system as in claim 24 further comprising a programmable circuit for programming which of said switch elements is selectively enabled.

26. A processor based system as in claim 15 wherein said output circuits are output buffer circuits.

27. A processor based system as in claim 15 wherein each of said output circuits receives and outputs a respective data signal from a memory array.

28. A processor based system as in claim 20 wherein said switch circuit comprises at least one multiplexor.

29. A memory device comprising:

a memory core; and

a data output apparatus coupled to said memory core and comprising:

a plurality of output circuits each of which receives and outputs a respective data signal from said core, each said output circuit operating in accordance with a respective applied clock signal;

a clock source for supplying a first clock signal;

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits.

30. A memory device as in claim 29 wherein each of said output circuits has an associated output data hold time, the timing of which is adjusted by the delay of a respective delay circuit.

31. A memory device as in claim 30 wherein the amount of delay applied by each of said adjustable delay circuits is programmable.

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32. A memory device as in claim 30 wherein the delay of each of said adjustable delay circuits is adjusted such that the timing of said data hold time of each of said output circuits is substantially coincident.

33. A memory device as in claim 30, further comprising a plurality of data output terminals respectively connected to said output circuits, and

wherein the delay of each of said adjustable delay circuits is adjusted such that the data hold time as seen at said respective output terminal is substantially coincident.

34. A memory device as in claim 29 wherein each of said delay circuits comprises:

an input for receiving said first clock signal;

a plurality of delay elements, each of said delay elements providing different respective delay to a signal applied thereto; and,

a switch circuit for selectively causing a selected one of said delay elements to delay said first clock signal and apply a delayed first clock signal to a respective output circuit.

35. A memory device as in claim 34 further comprising a programming circuit for programming said switch circuit to selectively apply said first clock signal to one of said delay elements.

36. A memory device s in claim 35 wherein said programming circuit comprises at least one fuse element.

37. A memory device as in claim 35 wherein said programming circuit comprises at lest one anti-fuse element.

38. A memory device as in claim 35 wherein said switch circuit comprises a plurality of switch elements respectively coupled to said plurality of delay elements, one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element.

39. A memory device as in claim 38 further comprising a programmable circuit for programming which of said switch elements is selectively enabled.

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40. A memory device as in claim 29 wherein said output circuits are output buffer circuits.

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41. A method of providing data output signals comprising:

receiving a plurality of data output signals at respective output circuits; and

operating said output circuits in response to respective applied clock signals to make said data output signals available at the output of said output circuits;

providing a first clock signal; and

generating each said respective applied clock signal from said first clock signal, each said respective applied clock signals having a respective adjustable delay relative to said first clock signal.

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42. A method as in claim 41 wherein said data output signals are available at the outputs of said output circuits for a respective data hold time, the timing of said data hold time for each of said output circuits being independently adjusted by adjusting the delay of a respective applied clock signal.

43. A method as in claim 42 wherein the amount of delay of each of said applied clock signals is programmable.

44. A method as in claim 42 further comprising adjusting the delay of each of said applied clock signals such that the timing of said data hold time of each of said output circuits is substantially coincident.

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45. A method as in claim 42, wherein each of said output circuits is connected to a respective output terminal, said method further comprising adjusting the delay of said applied clock signals such that the data hold time, as seen at each of said output terminals, is substantially coincident.

46. A method as in claim 45 wherein said terminals are exterior terminals of an integrated circuit package containing said output circuits.

47. A method as in claim 41 wherein each of said applied clock signals is generated by receiving said first clock signal and subjecting said received first clock signal to a selected one of a plurality of signal delays.

48. A method as in claim 47 wherein said selected one of said plurality of signal delays is programmable.

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